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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,126	12/15/2003	Ken A. Nishimura	10030571-1	5946

7590 07/10/2007  
AGILENT TECHNOLOGIES, INC.  
Legal Department, DL 429  
Intellectual Property Administration  
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EXAMINER

THOMAS, BRANDI N

ART UNIT	PAPER NUMBER
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2873

MAIL DATE	DELIVERY MODE
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07/10/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/737,126

Applicant(s)

NISHIMURA ET AL.

Examiner

Brandi N. Thomas

Art Unit

2873

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 10 April 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10, 12-18 and 20-26 is/are rejected.
- 7) ☒ Claim(s) 11 and 19 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☒ Other: Detailed Action.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10, 12-16, 20, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Bhuva et al. (5612713).

Regarding claim 1, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, comprising: memory elements (10a) configured to store data therein and shift data therebetween (col. 4, lines 35-40); and light modulation elements (10) respectively in communication with the memory elements (10a) (col. 2, lines 65-67 and col. 3, lines 1 and 2), wherein each of the light modulation elements (10) is alterable in response to the data stored in the respective corresponding memory elements (10a) (col. 3, lines 23-30).

Regarding claim 2, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said memory elements (10a) are arranged in an array having rows and columns (col. 4, lines 35-37).

Regarding claim 3, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said memory elements (10a) are configured to shift the data bi-directionally between rows (col. 4, lines 41-51).

Regarding claim 4, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said memory elements (10a) are configured to shift the data bi-directionally between columns (col. 4, lines 41-51).

Regarding claim 5, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said memory elements (10a) are configured to shift the data bi-directionally between at least one of non-adjacent rows and non-adjacent columns (col. 4, lines 41-51).

Regarding claim 6, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said memory elements (10a) are arranged in a nonorthogonal pattern (col. 4, lines 41-51).

Regarding claim 7, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said memory elements (10a) are static memory elements (col. 2, lines 53-55).

Regarding claim 8, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein each of the memory elements (10a) includes a feedback element (col. 4, lines 65-67 and col. 5, lines 1-5).

Regarding claim 9, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein the feedback element is a weak feedback element (col. 5, lines 1-5).

Regarding claim 10, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, further comprising access control elements (33) connected to said respective memory elements (10a) (col.4, lines 65-67).

Regarding claim 12, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein each of said memory elements (10a) further includes an output electrically coupled to an

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electrode (14) of said respective light modulation element (10) and to an input node of an additional one of said memory elements (10a) (col. 5, lines 6-16).

Regarding claim 13, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said memory elements (10a) are interconnected in a shift register (35) (col. 4, lines 35-40).

Regarding claim 14, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said memory elements (10a) each include a master-slave flip flop (col. 5, lines 8-10).

Regarding claim 15, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, further comprising: a timing circuit (clock) in communication with each of said memory elements (10a) to shift data between said memory elements (10a) (col. 4, lines 41-46).

Regarding claim 16, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said timing circuit comprises a ripple clock (col. 4, lines 41-46).

Regarding claim 20, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said light modulation elements (10) comprise micromirrors (21) (col. 3, line 66).

Regarding claim 21, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said memory elements (10a) are arranged in blocks (31) (col. 4, lines 53-55), a first one of said blocks (31) configured to receive data from an external input and the others of said blocks configured to receive data from other ones of said memory elements (10a) (figure 3).

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhuva et al. (5612713).

Regarding claim 17, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator but does not specifically disclose the light modulation elements comprising liquid crystal material. It would have been obvious to modify the invention to include liquid crystal material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use (In re Leshin, 125 USPQ 416). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention to include wherein the light modulation elements comprising liquid crystal material for the purpose of using a lithography system.

Regarding claim 18, Bhuva et al. discloses, in figures 2 and 3, a spatial light modulator, wherein said light modulation elements (10) further comprise: a common electrode (15) configured to receive a common electrode signal for said light modulation elements (10) (col. 3, lines 28-30); and a respective pixel electrode (14) configured to receive the data stored in said respective memory elements (10) (col. 3, lines 31-34).

5. Claims 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gale et al. (5285407) in view of (JP 07-177041).

Regarding claims 22 and 25, Gale et al. discloses, in figures 2A, 2B, and 3, a method for performing photolithography, said method comprising: altering ones of the light modulation

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elements (21) in response to the data loaded thereunto to transfer the image onto a substrate (col. 5, lines 9-12); shifting the data between memory elements (col. 4, lines 7-11, 17-24); altering ones of the light modulation elements (21) in response to the data shifted thereunto to transfer the image onto the substrate (col. 4, lines 7-11, 17-24) but does not specifically disclose loading data representing an image into memory elements in communication with respective light modulation elements. JP 07-177041 discloses, in figure 1, loading data representing an image into memory elements (43 and 44) in communication with respective light modulation elements (22) (sections 0019 and 0021). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the device of Gale with the modulation elements of JP 07-177041 for the purpose of displaying the stored and shifted data (sections 0019 and 0021).

Regarding claim 23, Gale et al. discloses, in figures 2A, 2B, and 3, a method for performing photolithography, wherein each said altering further comprises: applying a voltage in response to the data to the change optical characteristics of the light modulation elements (21) (col. 4, lines 44-61).

Regarding claim 24, Gale et al. discloses, in figures 2A, 2B, and 3, a method for performing photolithography, wherein said shifting further comprises: utilizing a ripple clock to control the timing of said shifting (col. 4, lines 13-16).

Regarding claim 26, Gale et al. discloses, in figures 2A, 2B, and 3, a method for performing photolithography, wherein said altering in response to the shifted data is performed after said moving (col. 5, lines 9-12).

*Allowable Subject Matter*

6. Claims 11 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The prior art taken either singularly or in combination fails to anticipate or fairly suggest the limitations of the independent claim(s), in such a manner that a rejection under 35 U.S.C. 102 or 103 would be proper. The prior art fails to teach a combination of all the claimed features as presented in claim(s) 11, wherein the claimed invention comprises, in claim 11, access control elements including a forward access control element and a reverse access control element; in claim 19, a timing circuit that shifts inverted data from a first to a second memory element and switches the common electrode signal, as claimed.

*Response to Arguments*

8. Applicant's arguments filed 4/10/07 have been fully considered but they are not persuasive. The applicant argues that the memory cells 10a are configured to "shift data therebetween" as recited in Claim 1. However, Bhuvra discloses that the memory elements include shift register (24), which inherently shifts data therebetween (col. 4, lines 35-40).

*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandi N. Thomas whose telephone number is 571-272-2341. The examiner can normally be reached on Monday - Thursday from 6-4:30.



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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Mack can be reached on 571-272-2333. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brandi N Thomas  
Examiner  
Art Unit 2873

  
BNT

  
RICKY MACK  
SUPERVISORY PATENT EXAMINER